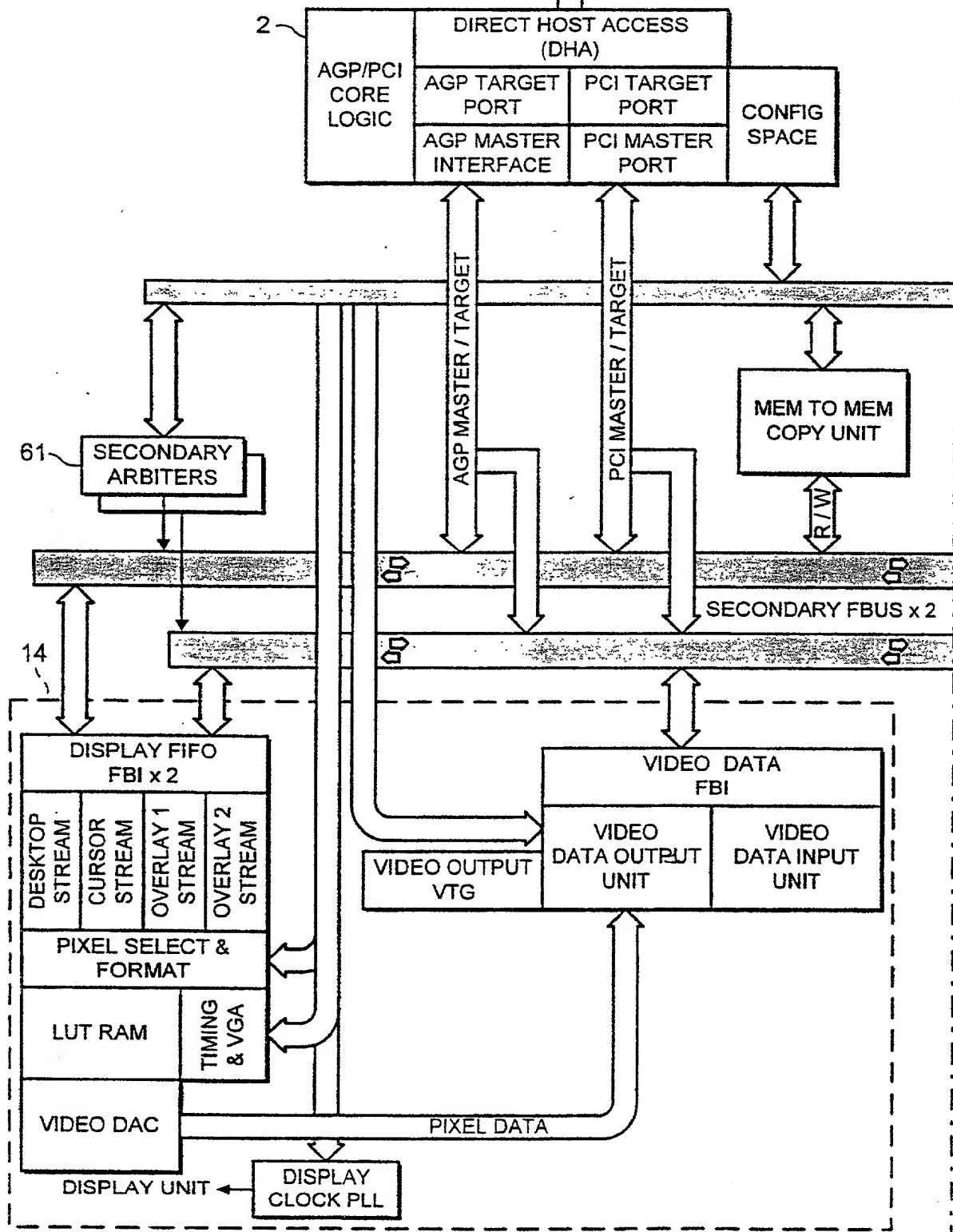


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FIG. 2(a)



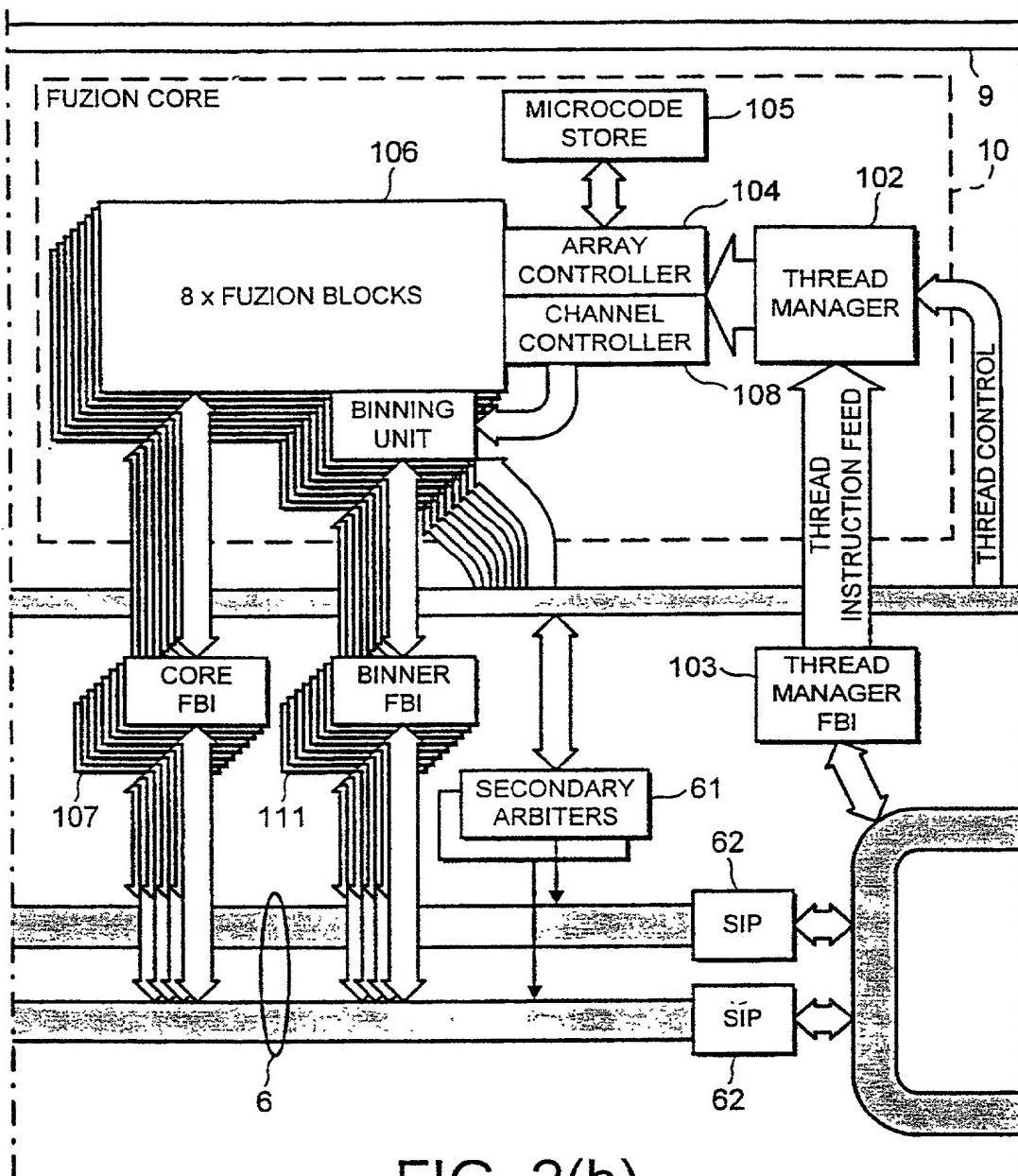


FIG. 2(b)

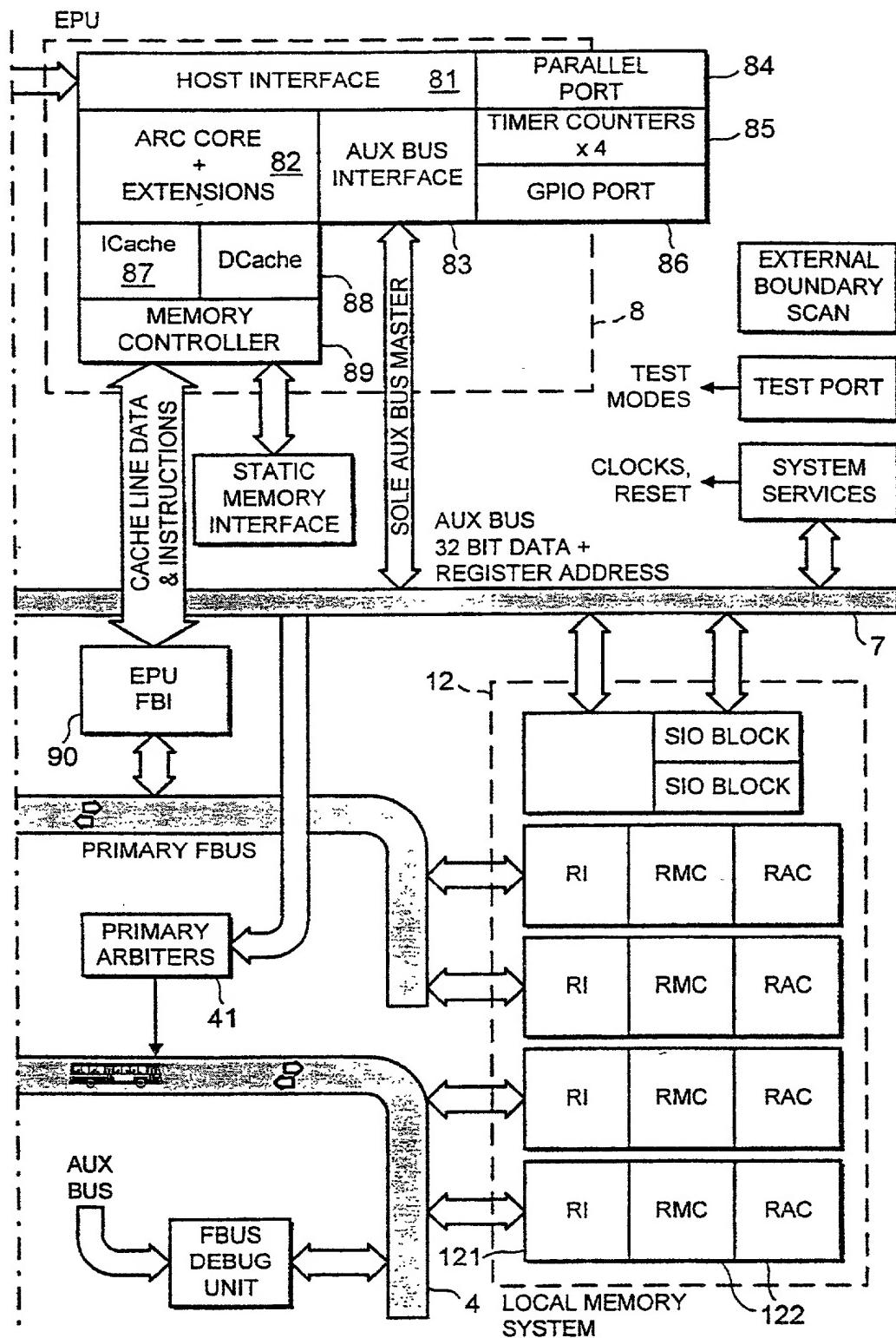


FIG. 2(c)

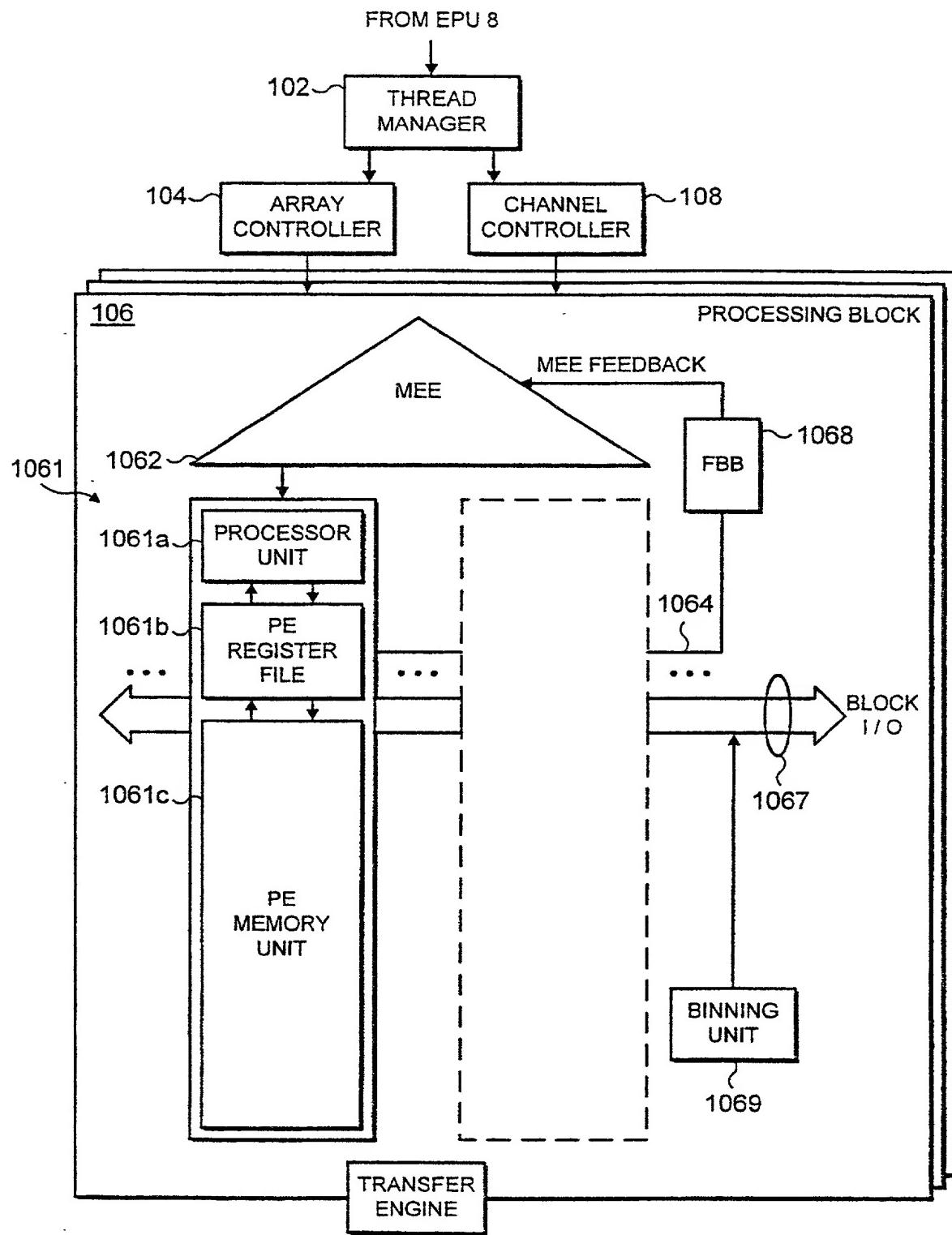


FIG. 3

**FIG. 4**

1023

The diagram illustrates the Thread Manager™ architecture. It consists of several main components:

- FETCH UNIT** (1023) connects to **I/F LOGIC** (1022).
- I/F LOGIC** (1022) provides **THREADS FROM EPU-CONTROLLED DMA** and **FLOW CONTROL PER THREAD**.
- TM CACHE** (1024) contains 8 slots labeled B0 through B7.
- SEMAPHORE CONTROLLER** (1028) manages **SEMAPHORE SIGNALS FROM EPU** (1034) and **SEMAPHORE INSTRUCTIONS**.
- STATUS BLOCK** (1030) receives **SEMAPHORE SIGNALS FROM EPU** (1034) and **SEMAPHORE INSTRUCTIONS**.
- SCHEDULER** (1025) manages **CONTROL & STATUS INTERFACE TO EPU** (1026).
- THREAD PROCESSOR** (1036) contains multiple parallel threads, indexed from 0 to 7.
- INSTRUCTIONS TO ARRAY CONTROLLER AND CHANNEL CONTROLLERS** (1032) are sent from the TM CACHE and the SEMAPHORE CONTROLLER.
- FLOW CONTROL FROM ARRAY CONTROLLER AND CHANNEL CONTROLLERS** (1031) is received by the TM CACHE.
- SEMAPHORE SIGNALS FROM ARRAY CONTROLLER AND CHANNEL CONTROLLERS** (1033) are sent from the TM CACHE to the SEMAPHORE CONTROLLER.

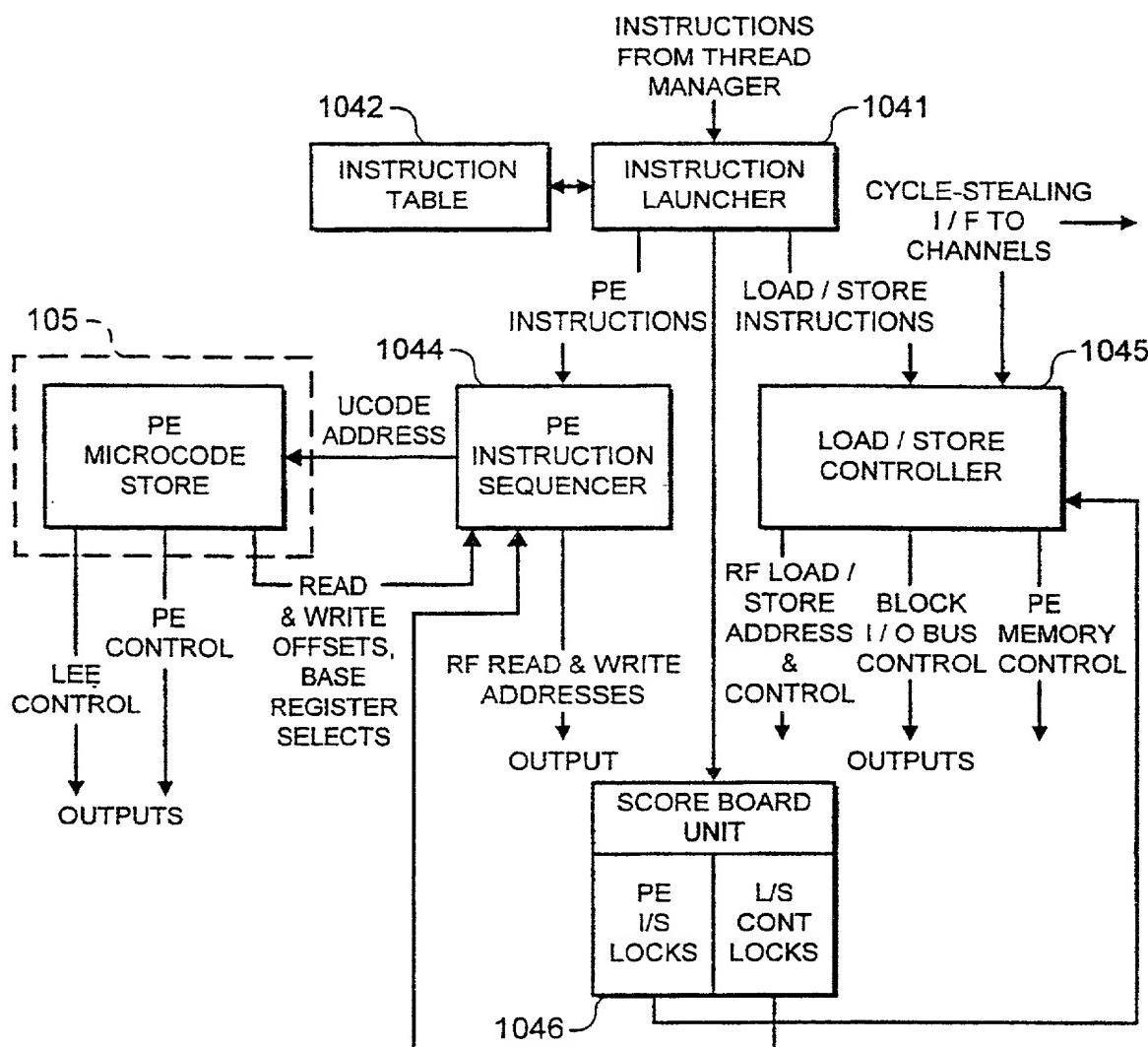


FIG. 5

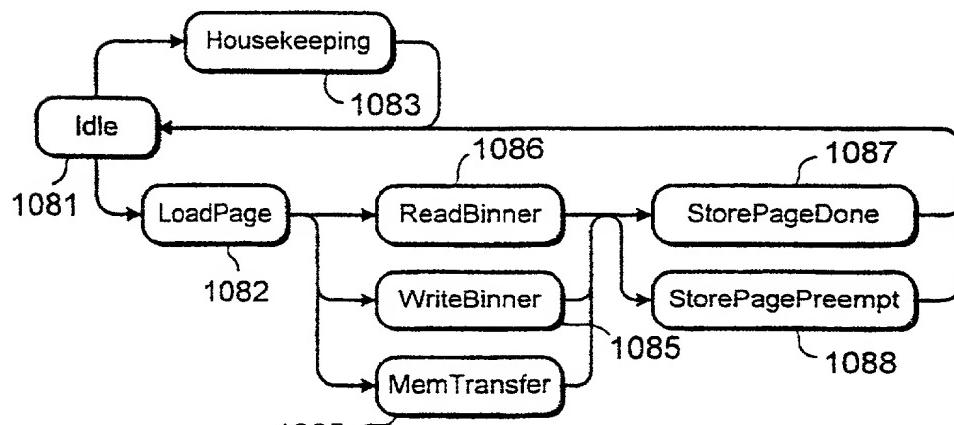


FIG. 6

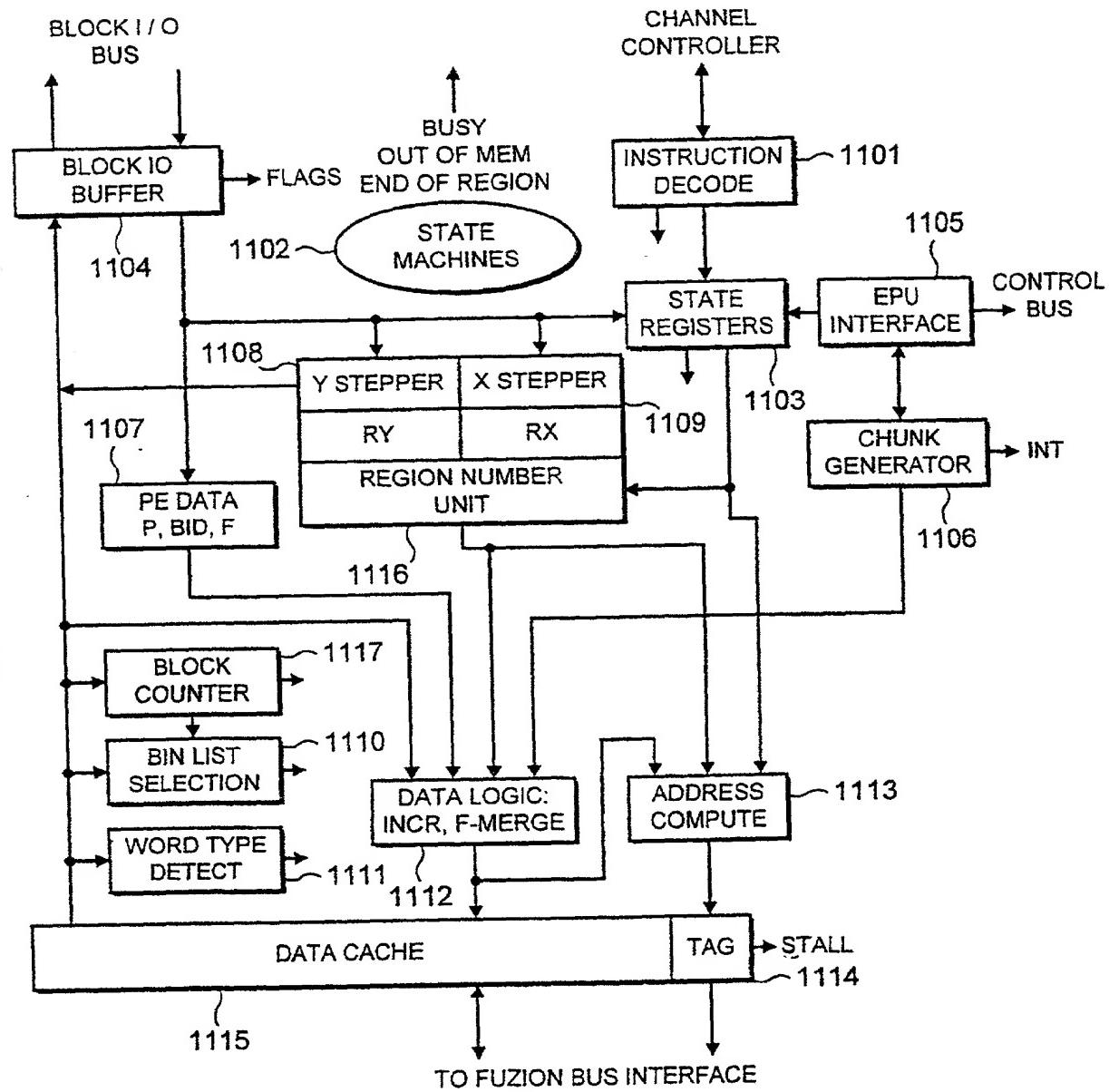


FIG. 7

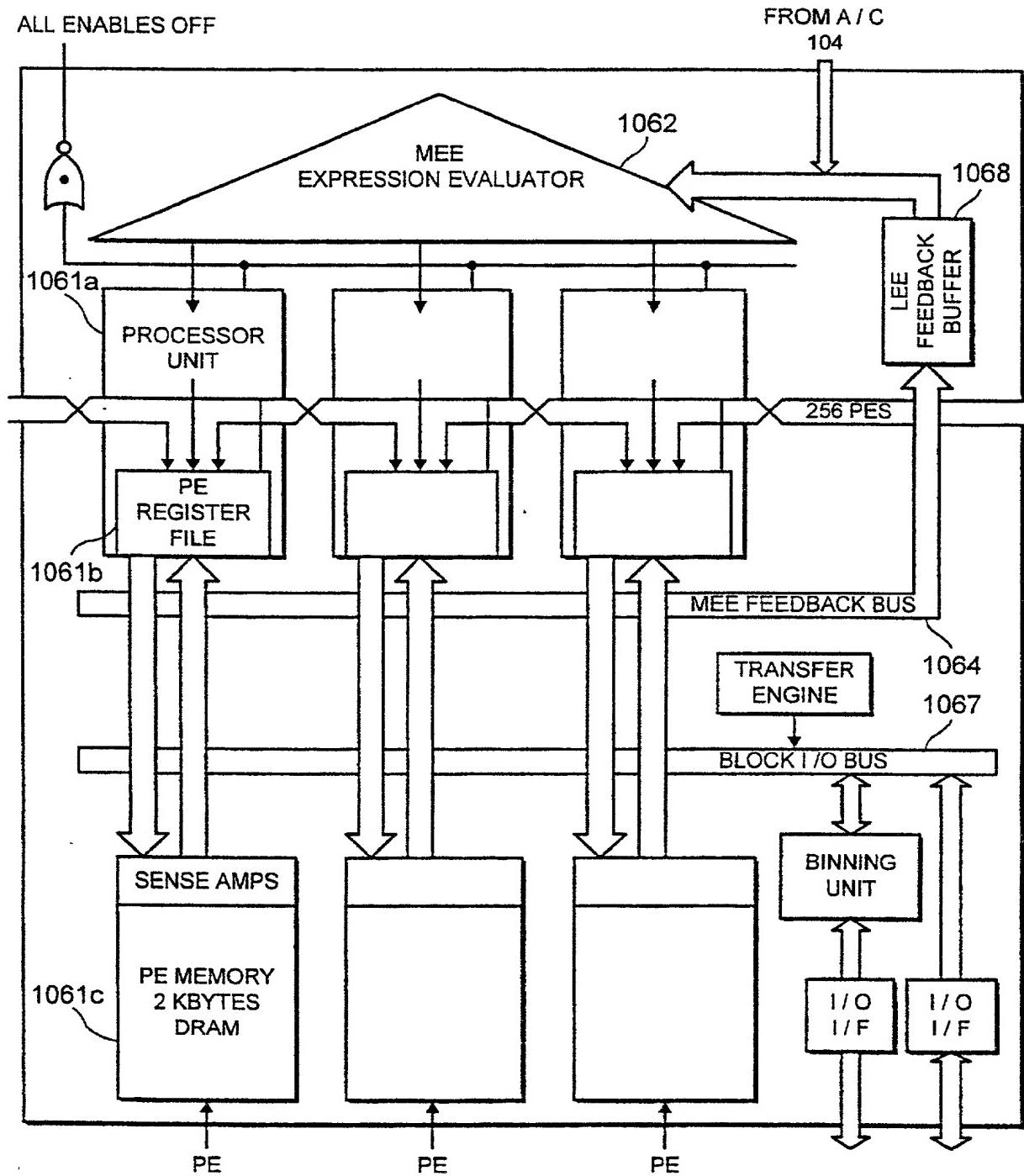


FIG. 8

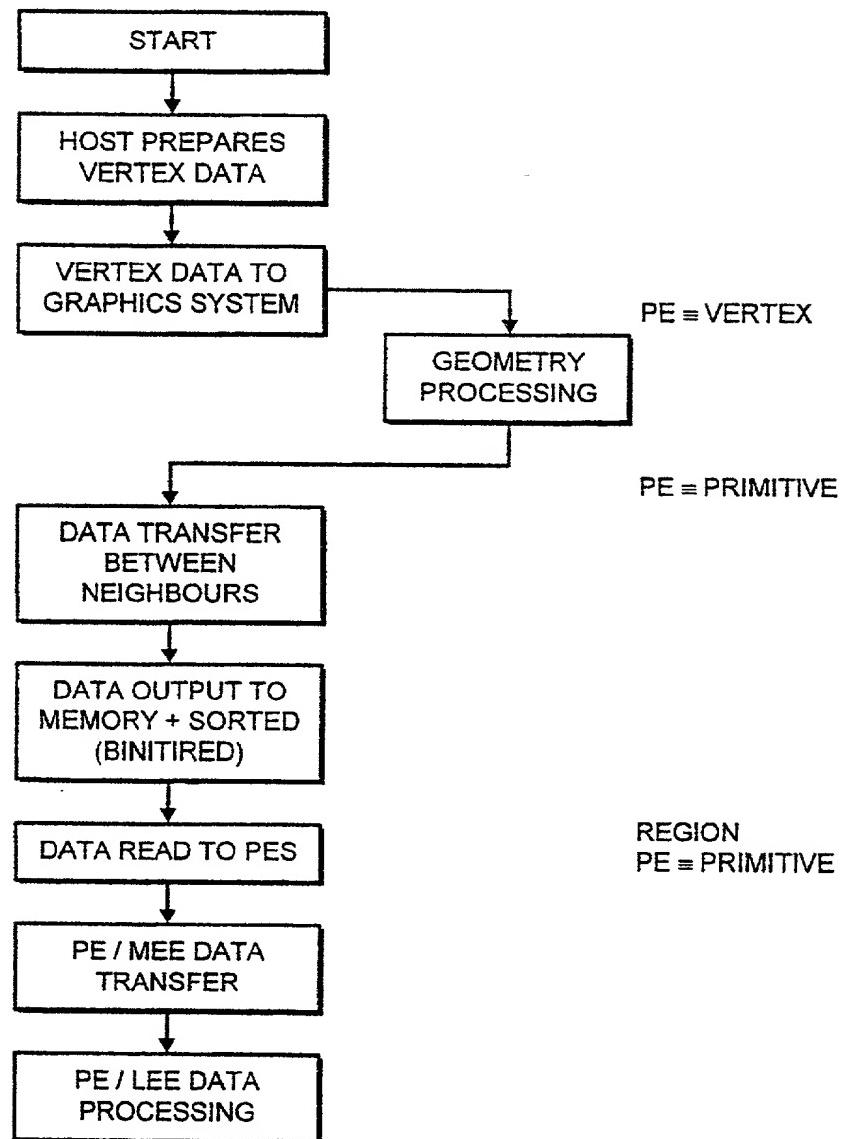
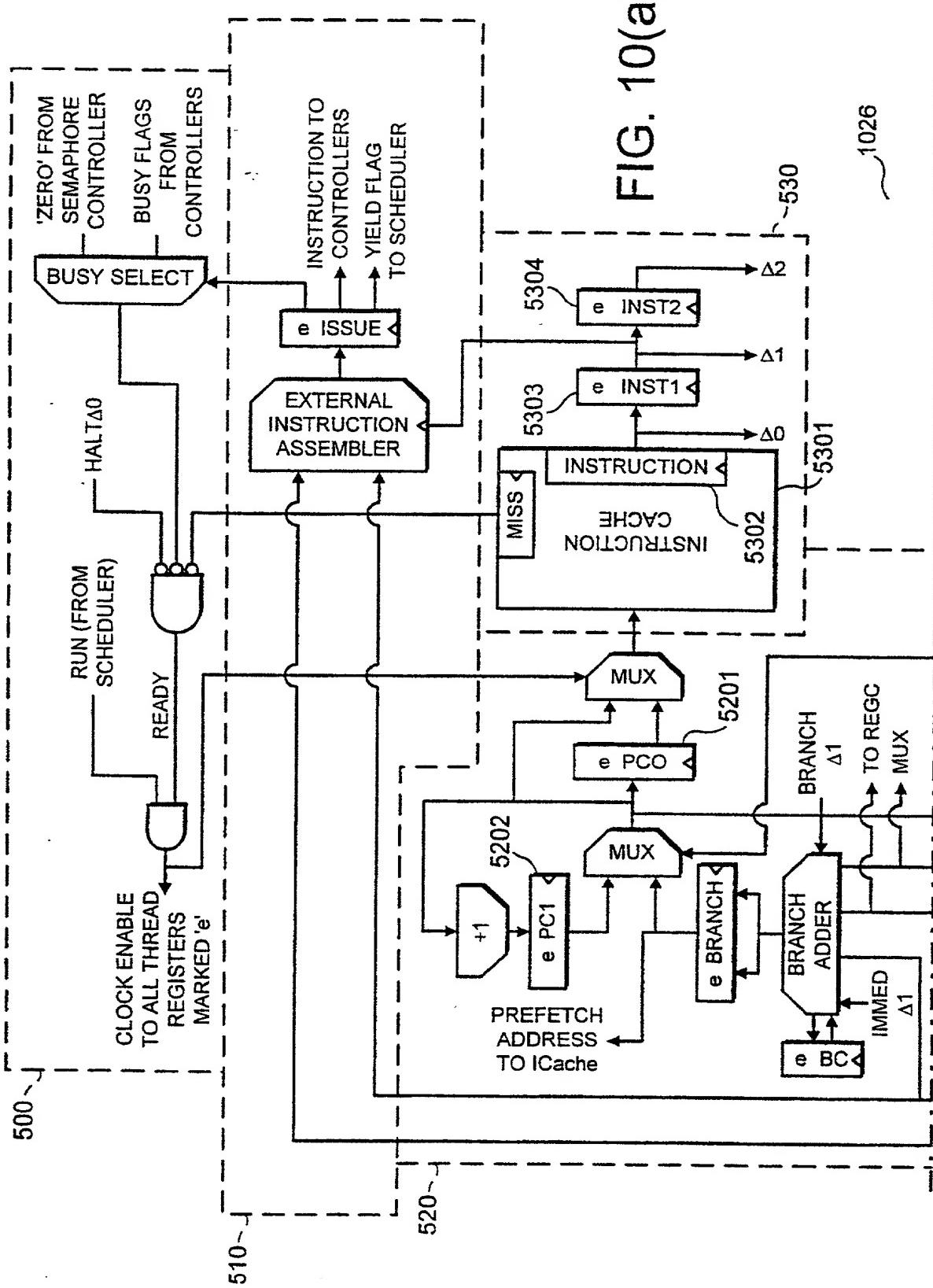


FIG. 9



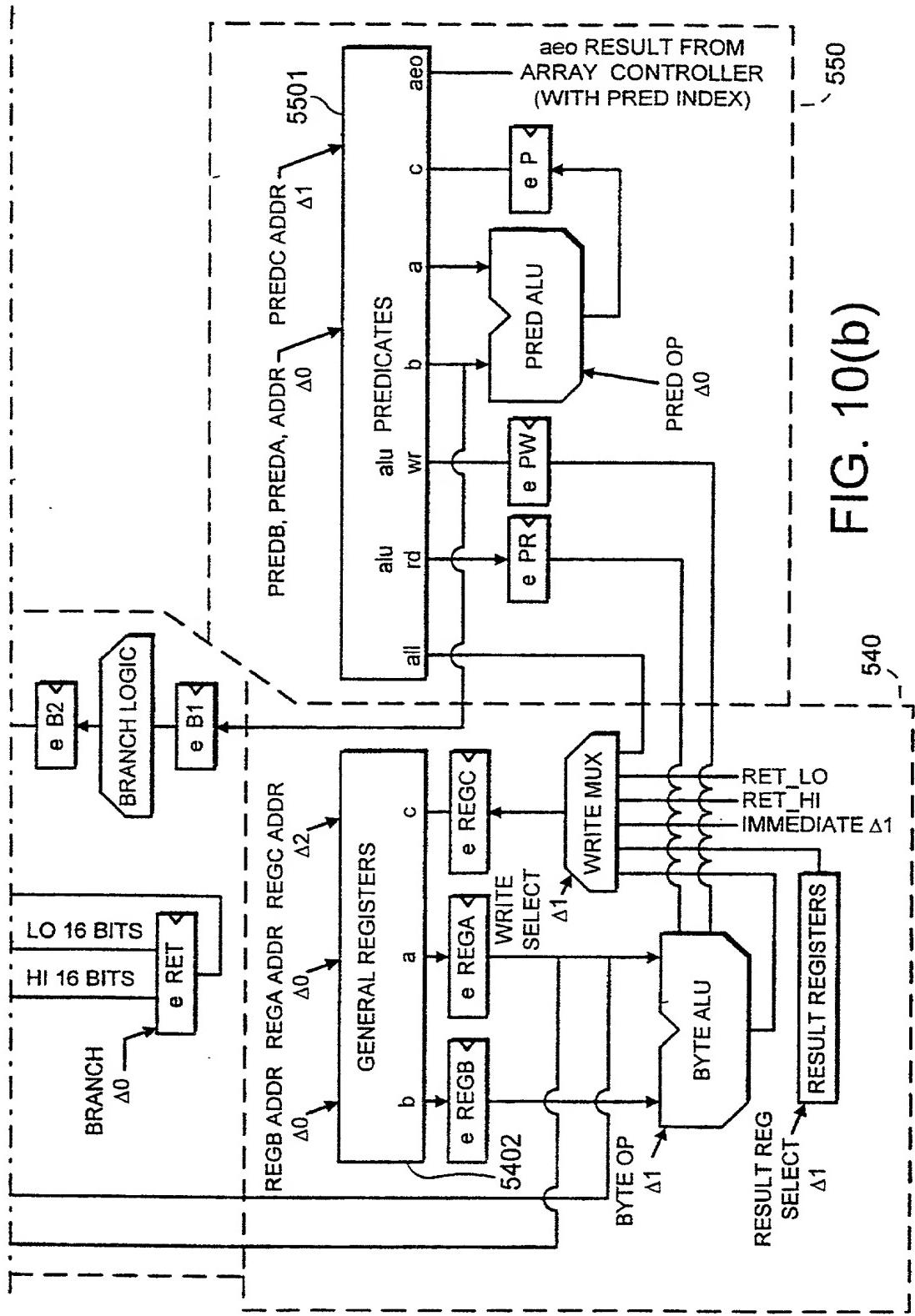


FIG. 10(b)

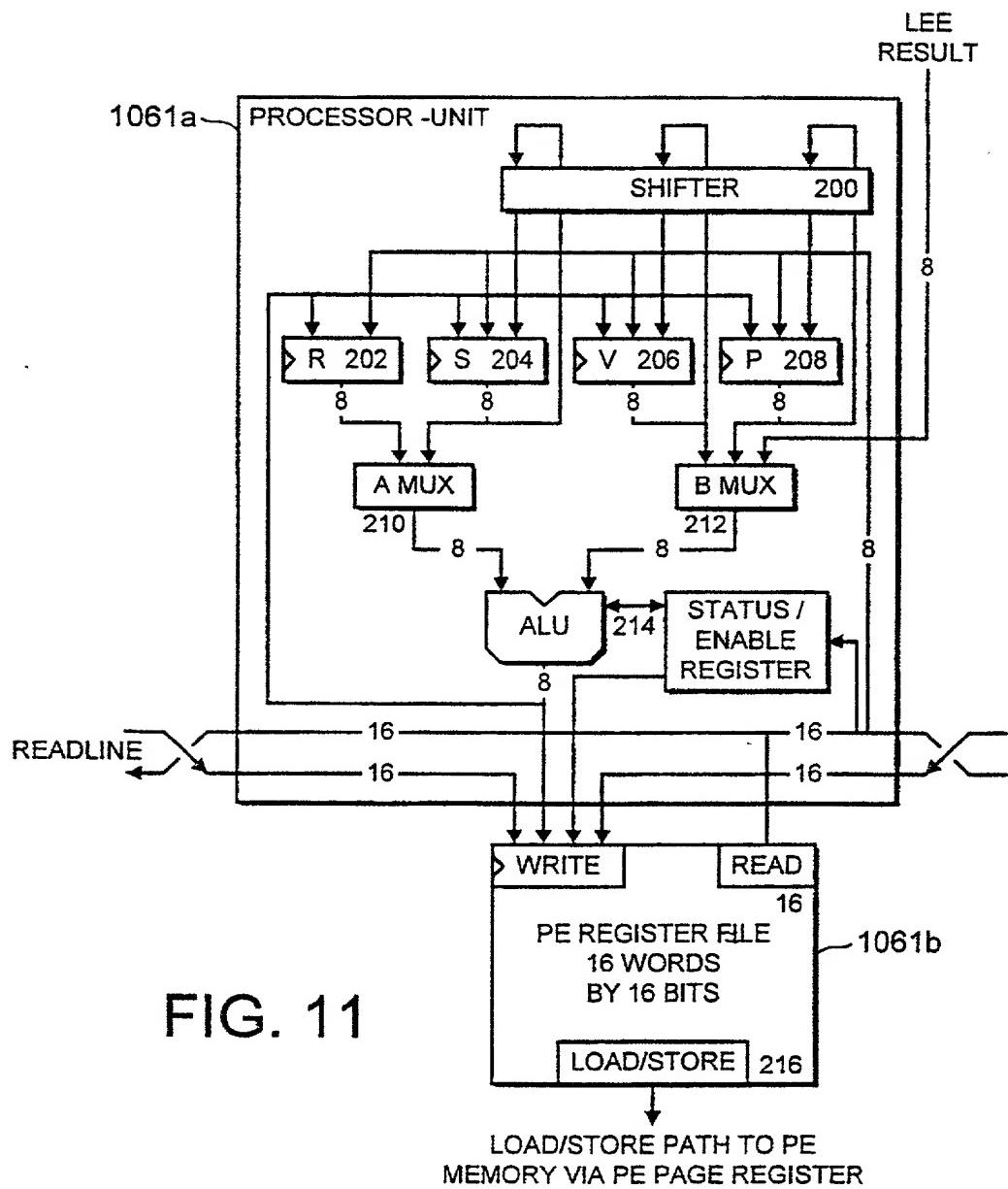


FIG. 11

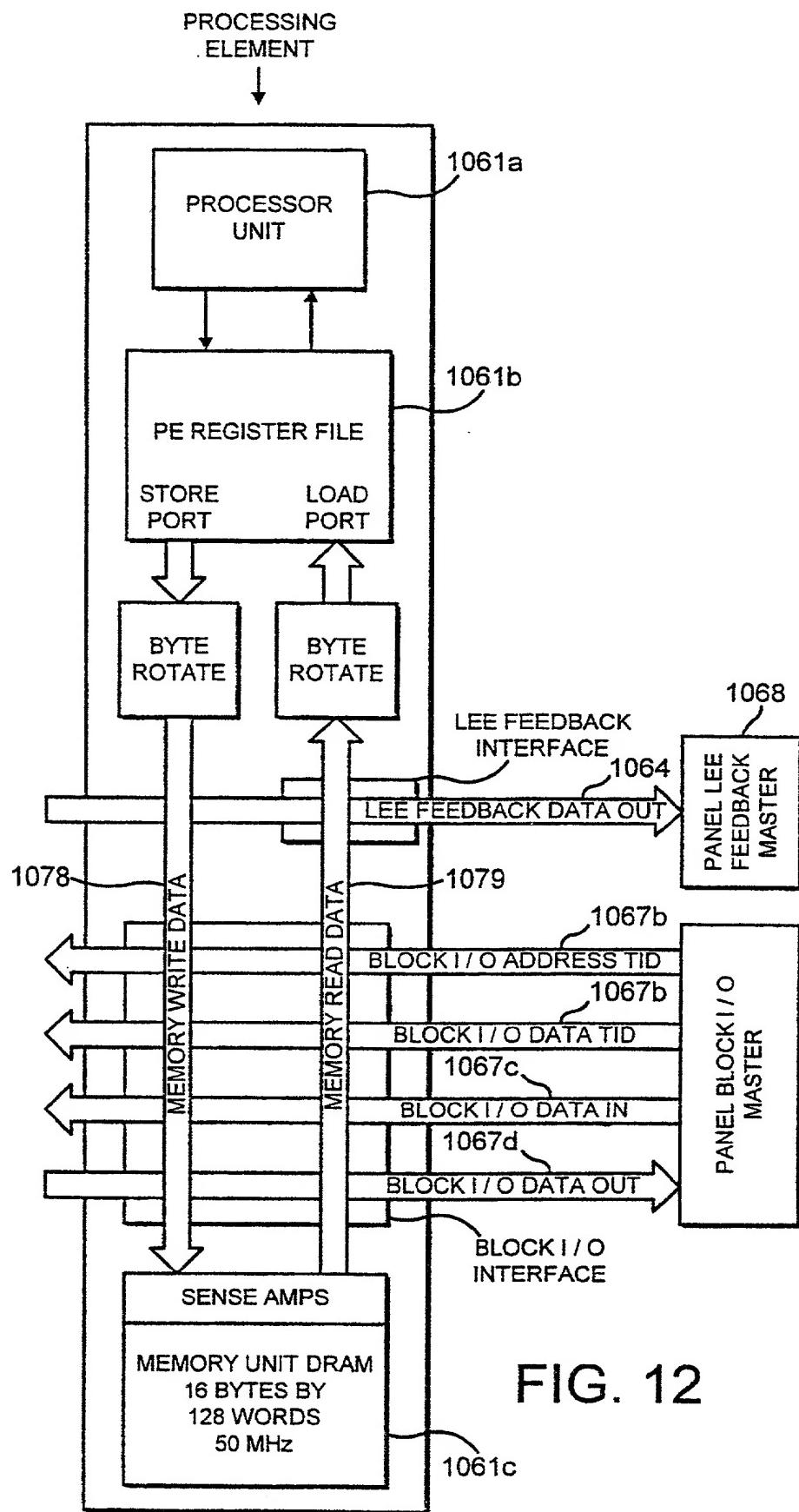


FIG. 12

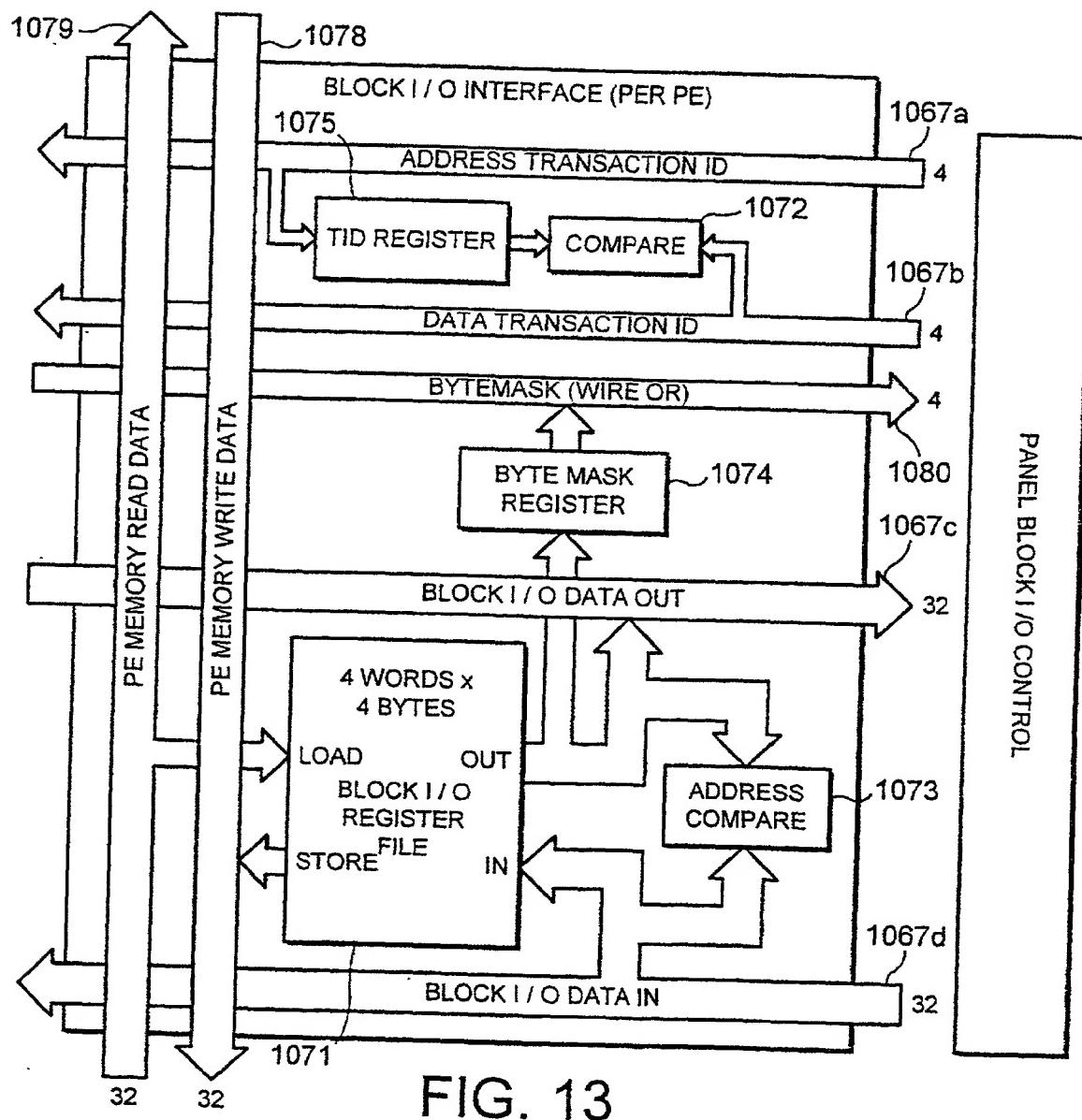


FIG. 13

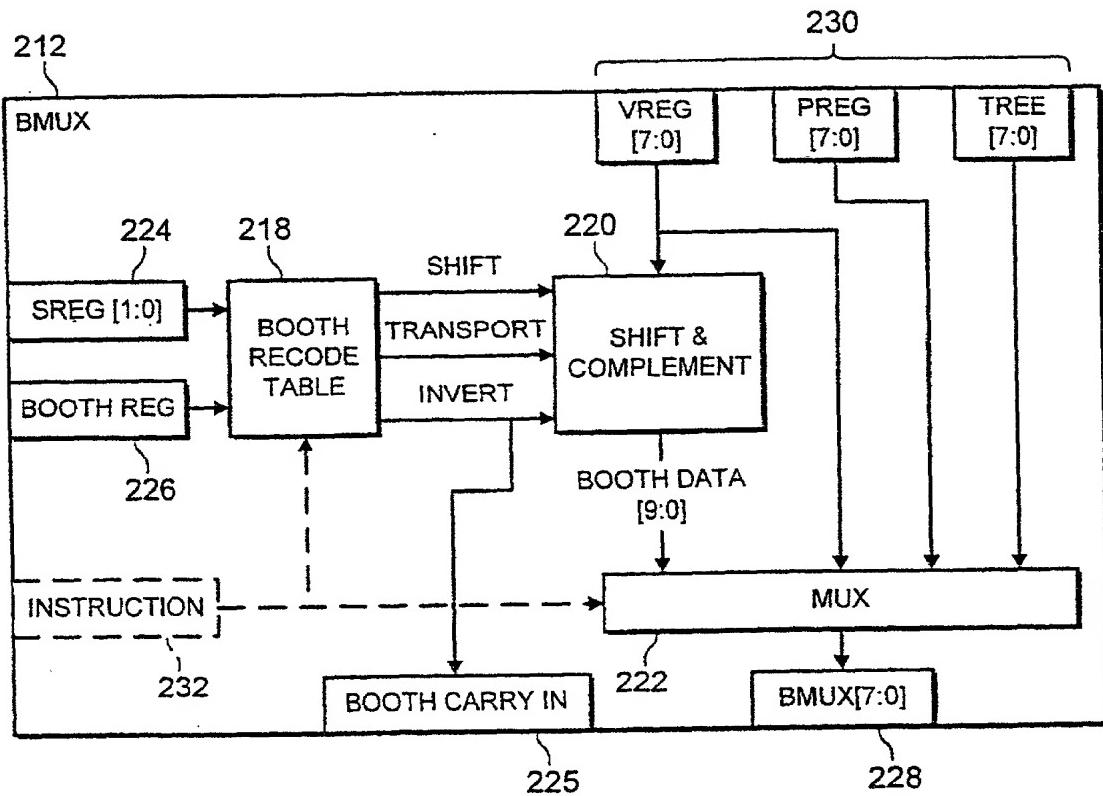


FIG. 14

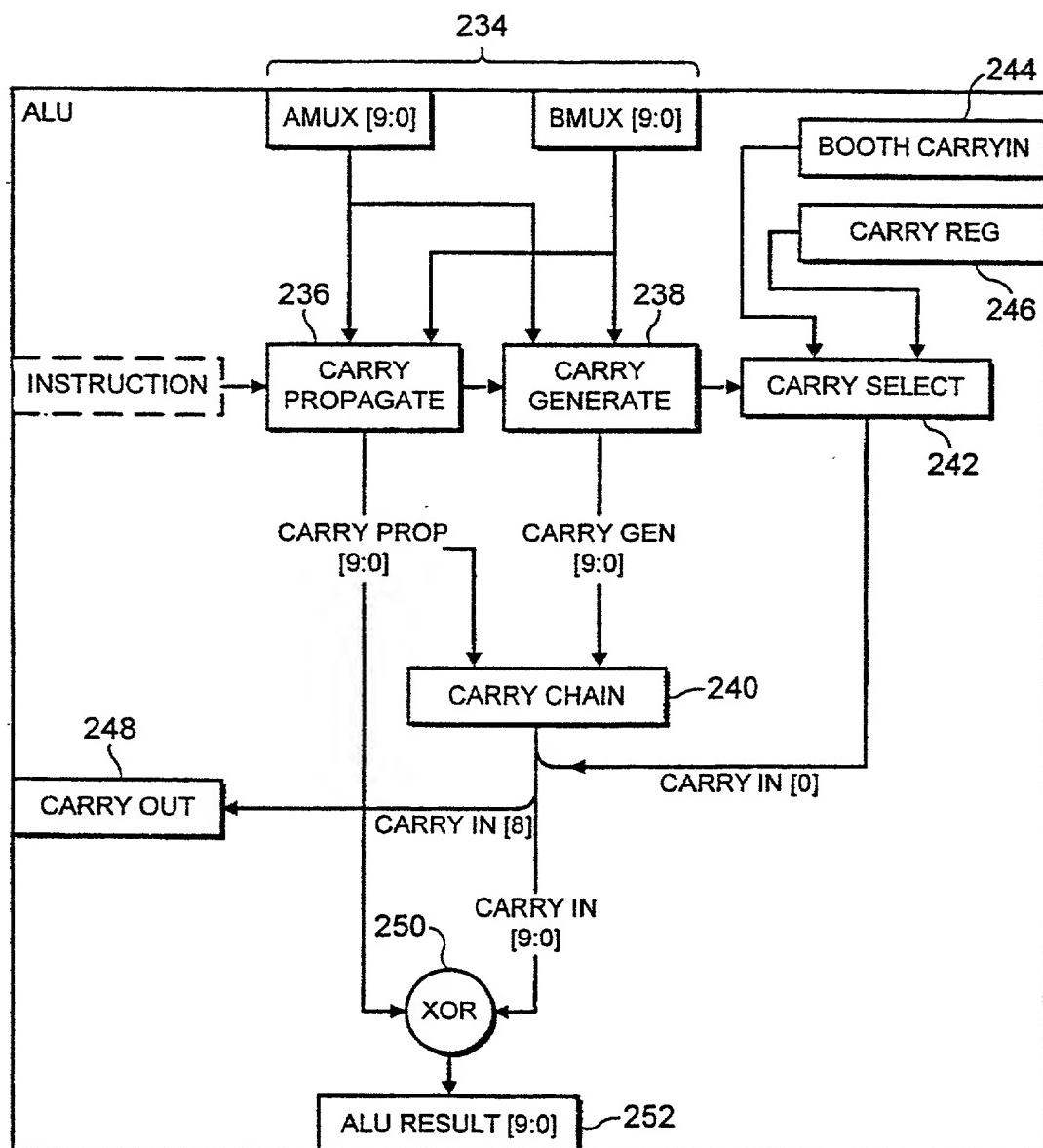


FIG. 15

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